



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/998,629	12/03/2001	John A. Morrison	10017862-1	7445
22879	7590	09/23/2004	EXAMINER	
HEWLETT PACKARD COMPANY P O BOX 272400, 3404 E. HARMONY ROAD INTELLECTUAL PROPERTY ADMINISTRATION FORT COLLINS, CO 80527-2400			YIGDALL, MICHAEL J	
			ART UNIT	PAPER NUMBER
			2122	

DATE MAILED: 09/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/998,629	Applicant(s) MORRISON ET AL.	
	Examiner Michael J. Yigdall	Art Unit 2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 December 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-20 are pending and have been examined. The priority date considered for the application is December 3, 2001.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-20 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-22 of copending Application No. 09/998,630. Although the conflicting claims are not identical, they are not

Art Unit: 2122

patentably distinct from each other because both recite analogous systems and methods for loading firmware in a high availability system.

For example, the limitations recited in claim 1 of the present application are recited in claim 1 of Application No. 09/998,630, where the mismatched cell is analogous to the first cell and the update cell is analogous to the second cell. Claim 8 of the present application similarly corresponds to claim 9 of Application No. 09/998,630. Likewise, the limitations recited in claim 15 of the present application are recited in claims 1 and 8 of Application No. 09/998,630.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-4 and 8-11 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pub. No. 2002/0091807 to Goodman (hereinafter “Goodman”).

With respect to claim 1, Goodman discloses a system for loading firmware in a high availability system (see the abstract) comprising:

(a) a high speed interconnect (see communication interface or interconnect 42 in FIG. 1, and page 2, first column, lines 10-17);

(b) a first cell coupled to the high speed interconnect and comprising errored firmware (see page 2, second column, lines 20-28 and 35-37, which shows a node or cell, i.e. a first cell, coupled to the interconnect having incompatible or errored firmware), the first cell configured to enable the high speed interconnect (see page 3, first column, lines 9-12, which shows that the cells enable communications over the interconnect); and

(c) a second cell coupled to the high speed interconnect and comprising update firmware (see page 2, second column, lines 29-35, which shows a node or cell, i.e. a second cell, coupled to the interconnect having updated firmware), the second cell configured to load the update firmware to the first cell via the high speed interconnect to replace the errored firmware (see page 3, second column, lines 8-20, which shows that the second cell loads the updated firmware to the first cell over the interconnect).

With respect to claim 2, Goodman further discloses the limitation wherein the second cell further is configured to reset the second cell and the first cell (see page 3, second column, lines 20-29, which shows resetting the nodes or cells).

With respect to claim 3, Goodman further discloses a third cell comprising second errored firmware (see page 2, second column, lines 20-28 and 35-37, which shows a node or cell, i.e. a third cell, coupled to the interconnect having incompatible or errored firmware), the third cell configured to enable the high speed interconnect (see page 3, first column, lines 9-12, which shows that the cells enable communications over the interconnect), wherein the first cell further

is configured to load the update firmware to the third cell via the high speed interconnect to replace the second errored firmware (see page 3, second column, lines 8-20, which shows loading the updated firmware to the cells over the interconnect).

With respect to claim 4, Goodman further discloses the limitation wherein the errored firmware comprises at least one member of a group consisting of firmware that is not a desired version of firmware and corrupt firmware (see page 3, first column, lines 36-42, which shows that the errored firmware comprises firmware that is not the latest version of firmware).

With respect to claim 8, Goodman discloses a method for loading firmware in a high availability system (see the title and abstract) comprising a high speed interconnect (see communication interface or interconnect 42 in FIG. 1, and page 2, first column, lines 10-17) and at least a first cell and a second cell, the first cell coupled to the high speed interconnect and comprising errored firmware such that the high speed interconnect is not enabled for the first cell (see page 2, second column, lines 20-28 and 35-37, which shows a node or cell, i.e. a first cell, coupled to the interconnect having incompatible or errored firmware, and lines 29-35, which shows that the first cell may be disabled, i.e. not enabled for the interconnect), the second cell coupled to the high speed interconnect and comprising update firmware (see page 2, second column, lines 29-35, which shows a node or cell, i.e. an update cell, coupled to the interconnect having updated firmware), the method comprising:

enabling the high speed interconnect by the first cell (see page 3, first column, lines 9-12, which shows the first cell enabling communications over the interconnect); and

Art Unit: 2122

loading update firmware from the second cell to the first cell via the high speed interconnect to replace the errored firmware (see page 3, second column, lines 8-20, which shows the second cell loading the updated firmware to the first cell over the interconnect).

With respect to claim 9, the limitations recited in the claim are analogous to the limitations recited in claim 2 (see the reasoning applied to claim 2 above).

With respect to claim 10, the limitations recited in the claim are analogous to the limitations recited in claim 3 (see the reasoning applied to claim 3 above).

With respect to claim 11, the limitations recited in the claim are analogous to the limitations recited in claim 4 (see the reasoning applied to claim 4 above).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 5-7 and 12-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodman, as applied to claims 1 and 8 above, respectively, in view of U.S. Pat. No. 6,334,177 to Baumgartner et al. (hereinafter "Baumgartner").

With respect to claim 5, although Goodman discloses a communication interface or interconnect used for both messages (see page 3, first column, lines 5-12) and firmware (see

Art Unit: 2122

page 3, second column, lines 8-20), Goodman does not expressly disclose a separate manageability system interconnect.

However, Baumgartner discloses a non-uniform memory access system having a plurality of nodes or cells (see the title and abstract) connected by a high-speed interconnect (see interconnect 16 in FIG. 1, and column 3, lines 13-19), and a manageability system interconnect (see bus 12 in FIG. 1, and column 3, lines 2-9), over which commands are transmitted (see column 5, lines 11-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the firmware update features of Goodman within the architecture taught by Baumgartner, in order automatically maintain compatible firmware among nodes (see Goodman, page 1, second column, lines 19-29) in a multiprocessor system that further provides speed advantages and simplified programming (see Baumgartner, column 1, lines 41-48).

Therefore, Goodman in view of Baumgartner further discloses:

a manageability system interconnect (see Baumgartner, bus or interconnect 12 in FIG. 1, and column 5, lines 11-13, which shows receiving commands or messages, i.e. manageability system commands, over the interconnect);

wherein the first cell is configured to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement via the manageability system interconnect and to enable the high speed interconnect (see Goodman, page 3, first column, lines 5-12, which shows the first cell receiving a code signature, i.e. an update message, and enabling communications over the interconnect, i.e. with an acknowledgement); and

Art Unit: 2122

wherein the second cell further is configured to activate an update menu, to receive an update command generated via the update menu (see Goodman, page 3, first column, line 53 to second column, line 3, which shows checking the code signature of each node, i.e. activating an update menu, and selecting a node from the menu to provide the update, i.e. generating an update command), and, in response thereto, to transmit the update message to the first cell and, after receiving the acknowledgment, to load the update firmware to the first cell via the high speed interconnect (see Goodman, page 3, second column, lines 8-20, which shows the second cell broadcasting or transmitting the firmware, i.e. an update message, to the first cell and subsequently loading the firmware over the interconnect).

With respect to claim 6, although Goodman discloses a communication interface or interconnect used for both messages (see page 3, first column, lines 5-12) and firmware (see page 3, second column, lines 8-20), Goodman does not expressly disclose a separate manageability system interconnect.

However, Baumgartner discloses a non-uniform memory access system having a plurality of nodes or cells (see the title and abstract) connected by a high-speed interconnect (see interconnect 16 in FIG. 1, and column 3, lines 13-19), and a manageability system interconnect (see bus 12 in FIG. 1, and column 3, lines 2-9), over which commands are transmitted (see column 5, lines 11-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the firmware update features of Goodman within the architecture taught by Baumgartner, in order automatically maintain compatible firmware among nodes (see

Art Unit: 2122

Goodman, page 1, second column, lines 19-29) in a multiprocessor system that further provides speed advantages and simplified programming (see Baumgartner, column 1, lines 41-48).

Therefore, Goodman in view of Baumgartner further discloses:

a manageability system interconnect (see Baumgartner, bus or interconnect 12 in FIG. 1, and column 5, lines 11-13, which shows receiving commands or messages, i.e. manageability system commands, over the interconnect);

wherein the first cell further is configured to receive an update message via the manageability system interconnect and, in response thereto, to enable the high speed interconnect (see Goodman, page 3, first column, lines 5-12, which shows the first cell receiving a code signature, i.e. an update message, and enabling communications over the interconnect); and

wherein the second cell further is configured to transmit the update message to the first cell and, thereafter, to automatically load the update firmware to the first cell via the high speed interconnect (see Goodman, page 3, second column, lines 8-20, which shows the second cell broadcasting or transmitting the firmware, i.e. an update message, to the first cell and subsequently loading the firmware over the interconnect).

With respect to claim 7, although Goodman discloses a communication interface or interconnect used for both messages (see page 3, first column, lines 5-12) and firmware (see page 3, second column, lines 8-20), Goodman does not expressly disclose a separate manageability system interconnect.

However, Baumgartner discloses a non-uniform memory access system having a plurality of nodes or cells (see the title and abstract) connected by a high-speed interconnect (see interconnect 16 in FIG. 1, and column 3, lines 13-19), and a manageability system interconnect

Art Unit: 2122

(see bus 12 in FIG. 1, and column 3, lines 2-9), over which commands are transmitted (see column 5, lines 11-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the firmware update features of Goodman within the architecture taught by Baumgartner, in order automatically maintain compatible firmware among nodes (see Goodman, page 1, second column, lines 19-29) in a multiprocessor system that further provides speed advantages and simplified programming (see Baumgartner, column 1, lines 41-48).

Therefore, Goodman in view of Baumgartner further discloses:

a manageability system interconnect (see Baumgartner, bus or interconnect 12 in FIG. 1, and column 5, lines 11-13, which shows receiving commands or messages, i.e. manageability system commands, over the interconnect);

wherein the first cell further is configured to receive an update message via the manageability system interconnect and, in response thereto, to transmit an acknowledgement and to enable the high speed interconnect (see Goodman, page 3, first column, lines 5-12, which shows the first cell receiving a code signature, i.e. an update message, and enabling communications over the interconnect, i.e. with an acknowledgement); and

wherein the second cell further is configured to transmit the update message to the first cell and, after receiving the acknowledgment, to automatically load the update firmware to the first cell via the high speed interconnect (see Goodman, page 3, second column, lines 8-20, which shows the second cell broadcasting or transmitting the firmware, i.e. an update message, to the first cell and subsequently loading the firmware over the interconnect).

With respect to claim 12, the limitations recited in the claim are analogous to the limitations recited in claim 5 (see the reasoning applied to claim 5 above).

With respect to claim 13, the limitations recited in the claim are analogous to the limitations recited in claim 6 (see the reasoning applied to claim 6 above).

With respect to claim 14, the limitations recited in the claim are analogous to the limitations recited in claim 7 (see the reasoning applied to claim 7 above).

With respect to claim 15, Goodman discloses a system for updating firmware in a high availability system (see the abstract).

Although Goodman discloses a communication interface or interconnect used for both messages (see page 3, first column, lines 5-12) and firmware (see page 3, second column, lines 8-20), Goodman does not expressly disclose a separate manageability system interconnect.

However, Baumgartner discloses a non-uniform memory access system having a plurality of nodes or cells (see the title and abstract) connected by a high-speed interconnect (see interconnect 16 in FIG. 1, and column 3, lines 13-19), and a manageability system interconnect (see bus 12 in FIG. 1, and column 3, lines 2-9), over which commands are transmitted (see column 5, lines 11-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the firmware update features of Goodman within the architecture taught by Baumgartner, in order automatically maintain compatible firmware among nodes (see Goodman, page 1, second column, lines 19-29) in a multiprocessor system that further provides speed advantages and simplified programming (see Baumgartner, column 1, lines 41-48).

Therefore, Goodman in view of Baumgartner further discloses:

(a) a high speed interconnect (see Goodman, communication interface or interconnect 42 in FIG. 1, and page 2, first column, lines 10-17);

(b) a manageability system interconnect (see Baumgartner, bus or interconnect 12 in FIG. 1, and column 5, lines 11-13, which shows receiving commands or messages, i.e. manageability system commands, over the interconnect);

(c) a mismatched cell coupled to the high speed interconnect and comprising errored firmware (see Goodman, page 2, second column, lines 20-28 and 35-37, which shows a node or cell, i.e. a mismatched cell, coupled to the interconnect having incompatible or errored firmware), the mismatched cell configured to receive an update message via the manageability system interconnect and, in response thereto, to enable the high speed interconnect (see Goodman, page 3, first column, lines 5-12, which shows the mismatched cells receiving a code signature, i.e. an update message, and enabling communications over the interconnect); and

(d) an update cell coupled to the high speed interconnect and comprising update firmware (see page 2, second column, lines 29-35, which shows a node or cell, i.e. an update cell, coupled to the interconnect having updated firmware), the update cell configured to transmit the update message to the mismatched cell and to automatically load the update firmware to the mismatched cell via the high speed interconnect (see Goodman, page 3, second column, lines 8-20, which shows the update cell broadcasting or transmitting the firmware, i.e. an update message, to the mismatched cells and subsequently loading the firmware over the interconnect).

With respect to claim 16, Goodman in view of Baumgartner further discloses a second mismatched cell comprising second errored firmware (see Goodman, page 2, second column,

Art Unit: 2122

lines 20-28 and 35-37, which shows a node or cell, i.e. a second mismatched cell, coupled to the interconnect having incompatible or errored firmware), the second mismatched cell configured to receive a second update message via the manageability system interconnect and, in response thereto, to enable the high speed interconnect (see Goodman, page 3, first column, lines 5-12, which shows the mismatched cells receiving a code signature, i.e. a second update message, and enabling communications over the interconnect), wherein the update cell further is configured to transmit the second update message to the second mismatched cell and to automatically load the update firmware to the second mismatched cell via the high speed interconnect (see Goodman, page 3, second column, lines 8-20, which shows the update cell broadcasting or transmitting the firmware, i.e. a second update message, to the mismatched cells and subsequently loading the firmware over the interconnect).

With respect to claim 17, Goodman in view of Baumgartner further discloses the limitation wherein the update cell is configured to automatically load the update firmware to the mismatched cell only if an auto update flag is set (see Goodman, page 3, first column, lines 43-51, which shows setting a parameter or update flag, and line 65 to second column, line 6, which shows loading the code, i.e. the update firmware, only if indicated, i.e. by the flag).

With respect to claim 18, Goodman in view of Baumgartner further discloses the limitation wherein the update cell further comprises flash ROM configured to store the update firmware (see Goodman, page 2, first column, lines 47-55, which shows that the nodes or cells comprise flash memory for storing the firmware) and NVRAM configured to store a setting of the auto update flag (see Goodman, page 3, first column, lines 43-51, which shows storing the

Art Unit: 2122

flag in RAM, and page 2, first column, lines 47-55, which shows that the RAM may be battery backed-up RAM, i.e. NVRAM).

With respect to claim 19, Goodman in view of Baumgartner further discloses the limitation wherein the update cell further comprises at least one processor configured to process the update firmware (see Goodman, page 2, first column, lines 45-57, which shows that the nodes or cells comprise processors, i.e. for processing the firmware).

With respect to claim 20, Goodman in view of Baumgartner further discloses the limitation wherein the mismatched cell further is configured to transmit an acknowledgment via the manageability system interconnect after receiving the update message and the update cell further is configured to transmit the update firmware to the mismatched cell via the high speed interface after receiving the acknowledgement (see Goodman, page 3, second column, lines 8-20, which shows the mismatched cells transmitting a request, i.e. an acknowledgement to the update message, and the update cell transmitting the updated firmware over the interconnect).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. U.S. Pat. No. 6,055,632 to Deegan et al. discloses a method and apparatus for transferring firmware to a non-volatile memory of a programmable controller system.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdal whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

Art Unit: 2122

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.


After October 25, 2004, the examiner can be reached at (571) 272-3707, and the examiner's supervisor, Tuan Q. Dam can be reached at (571) 272-3694.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2122

mjy


TUAN DAM
SUPERVISORY PATENT EXAMINER